

IN THE CLAIMS

1. (Original) A method for conserving power for operating an M row x N column array of processor cells, comprising:
providing a row mask signal configured to enable selected cells in each row of the array;
providing a column mask signal configured to enable selected cells in each column of the array; and
gating the row mask signal and column mask signal with a clock signal of each cell to activate, at the next clock cycle, the enabled cells in the array based on the row mask signal and column mask signal.
2. (Original) The method of claim 1, further comprising broadcasting a context instruction to each enabled cell.
3. (Original) The method of claim 2, further comprising executing, during the clock cycle, the context instruction with only the activated cells in the array.
4. (Original) The method of claim 1, further comprising updating the row mask signal and the column mask signal during each clock cycle.
5. (Currently Amended) A method for saving power in an MxN array of processor cells, wherein each cell is configured to execute a context instruction when active, the method comprising:
masking ~~the~~ an MxN array of processor cells to enable a subset of cells of the array;
activating each enabled cell to execute the context instruction; and
disabling each unmasked cell in the array, such that each disabled cell does not consume power.
6. (Original) A power-saving arrangement for an MxN array of processor cells, comprising:
a row mask register configured to provide a row mask signal for enabling selected cells in each row of the array;
a column mask register configured to provide a column mask signal for enabling selected cells in each column of the array; and

a clock circuit, connected to supply each cell with a clock signal, each clock signal being gated with the row mask signal and column mask signal to activate the enabled cells upon a new clock cycle.

7. (Original) The arrangement of claim 6, wherein the row mask register is an M-bit register.

8. (Original) The arrangement of claim 6, wherein the column mask register is an N-bit register.

9. (Original) The arrangement of claim 6, further comprising a mask generator for generating a mask signal to the row mask register and the column mask register.

10. (Original) The arrangement of claim 6, further comprising a context instruction generator for generating and supplying a context instruction to each enabled cell for execution when the cell is activated.

11. (Original) A power saving arrangement for an MxN array of processor cells, comprising:

a mask circuit for generating a mask signal for masking a portion of the cells in the array;
and

a clock for providing a clock signal, the clock signal being gated with the mask signal to activate the masked cells upon a new clock cycle.

12. (Original) The arrangement of claim 11, wherein the mask circuit further comprises:

a row mask register connected to each row of cells; and

a column mask register connected to each column of cells.

13. (Original) The arrangement of claim 12, wherein the mask signal includes an M-bit row mask signal and an N-bit column mask signal.

14. (Original) The arrangement of claim 13, wherein the row mask signal and column mask signal are gated together at an input to each cell.

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15. (Original) The arrangement of claim 11, wherein the mask signal is configured to enable the masked cells.
